User Manual

for the Motherboard:

KT690/mITX

Preliminary

Document revision history.

Revision	Date	By	Comment
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- CPU Board
  1. Type.
  2. Part-number.
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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1. Introduction

This manual describes the KT690/mITX board made by KONTRON Technology A/S. The board will also be denoted KT690 family if no differentiation is required.

All boards are to be used with the Mobile AMD Sempron™ and AMD Turion™ 64 X2 Mobile Processors for S1 socket.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KT690 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 3 before switching-on the power.

2. Installation procedure

2.1 Installing the board

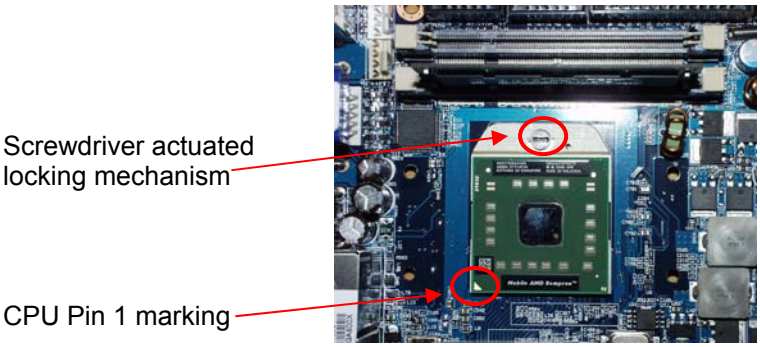
To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has CPU, DDR2 DRAM and Cooler mounted. In this case Step 2-4 can be skipped.

1. Turn off the power supply

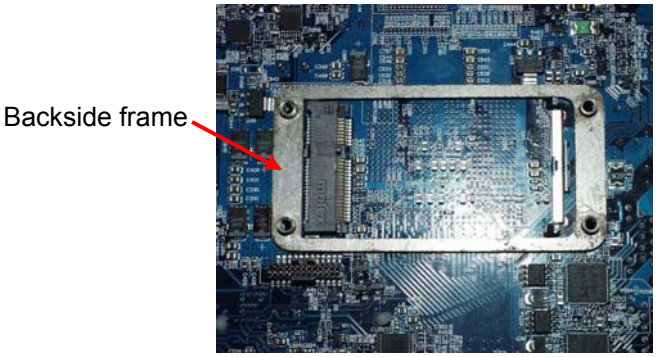
Warning: Do not use Power Supply without 3.3V monitoring watchdog, which is standard feature in ATX Power Supplies.
Running the board without 3.3V connected will damage the board after a few minutes.

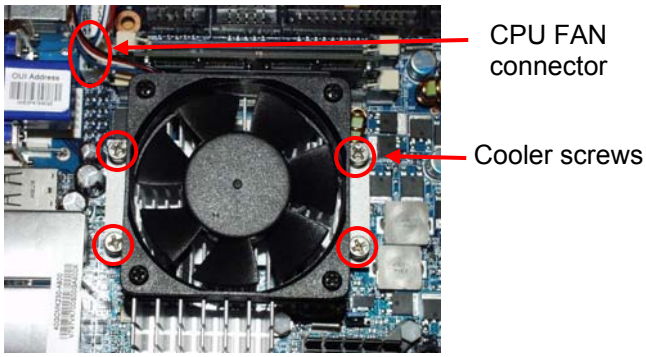
2. Insert the DDR2 SODIMM 200pin DRAM module(s)
Push down the module from the top side until the tabs lock. For a list of approved DDR2 SODIMM modules contact your Distributor or FAE.
DDR2-667 SODIMM 200pin DRAM modules (PC5300) are supported.

3. Install the processor
The CPU is keyed and will only mount in the CPU socket in one way. Use a 6mm flatheaded screwdriver to open/ close the CPU socket. The Mobile AMD Sempron™ and AMD Turion™ 64 X2 Mobile Processors for S1 socket are supported, refer to supported processor overview for details.



4. Cooler Installation
On the board backside, place frame with thread pointing away from the board. Place insulator material between board and frame. Use the 4 screws to lock the cooler from the topside; make sure to align the cooler even with the board. Connect the Fan electrically to the CPU FAN connector.





5. Connecting Interfaces
Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings to flat panel support.

6. **Connect Power supply**
   Connect power supply to the board by the ATX/ BTXPWR and 4-pin ATX connectors. For board to operate connection of both the ATX/BTX and 4-pin ATX (12V) connectors are required.

7. **Turn on the power on the ATX/ BTX power supply**

8. **Power Button**
   The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A “normally open” switch can be connected via the FRONTPNL connector.

9. **BIOS Setup**
   Enter the BIOS setup by pressing the <Del> key during boot up. Refer to the “BIOS Configuration / Setup“ section of this manual for details on BIOS setup.
   Enter Advanced Menu / CPU Configuration / Intel SpeedStep Tech. and set this option to “Maximum Performance”.

Note: To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

2.2 Requirement according to EN60950

Users of KT690 boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Component main data

The table below summarises the features of the KT690 embedded motherboard.

Form factor	KT690/mITX: mini ITX (170.18millimeters by 170.18millimeters)
Processor	• Support for Mobile AMD Sempron™, AMD Turion™ 64 and AMD Turion™ 64 X2 Mobile Processors for S1 socket • 35W maximum TDP • 1.6GT/s HyperTransport™ link, 800 MHz, 16bit/16bit • Hypertransport™ 1.0 Tunnel (I/O Bus) speed of 800MHz • Internal L1 cache of 128KB (Single core CPUs) / 128KB x2 (Dual core CPUs) • Internal L2 cache of 128/256/512KB (Single core CPUs) / 512KB x2 (Dual core CPUs) • Processor technology of 65nm / 90nm • DDR2 memory controller and bus interface
Memory	• Dual Channel DDR2 memory architecture • 2 pcs DDR2 SODIMM 200pin DRAM sockets onboard. • Support for DDR 533/667MHz unbuffered memory (PC2-4200/PC2-5300) • Support system memory from 256MB and up to 4GB/ 32GB* (* Memory modules for support of up to 32GB may not be available) • ECC not supported
Chipset	AMD Chipset consisting of: • AMD M690T northbridge (graphics tunnel) • ATI SB600 southbridge (I/O hub)
Video	• Integrated ATI Radeon™ X1200 graphics core o CRT Out connector o DVI-D connector (Digital only) o Onboard LVDS connector o TV-Out connector** • Dual independent pipe support: Mirror and Dual Independent displays supported. • Full DirectX® 9.0 support • Maximum resolution of 2048x1536 @ 32bpp for a maximum pixel clock speed of 400MHz. • LVDS interface supports dual channel, 24bit OpenLDI/ SPWG panels. • AMD HyperMemory allowing up to 256MB dynamically allocated Video Memory (System memory is allocated when it is needed).
Audio	Audio, 7.1 and 7.2 Channel High Definition Audio Codec using the Realtek ALC888 codec • Line-out • Line-in • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1, MIC2 • CDROM in • SPDIF Interface Onboard speaker

(continues)

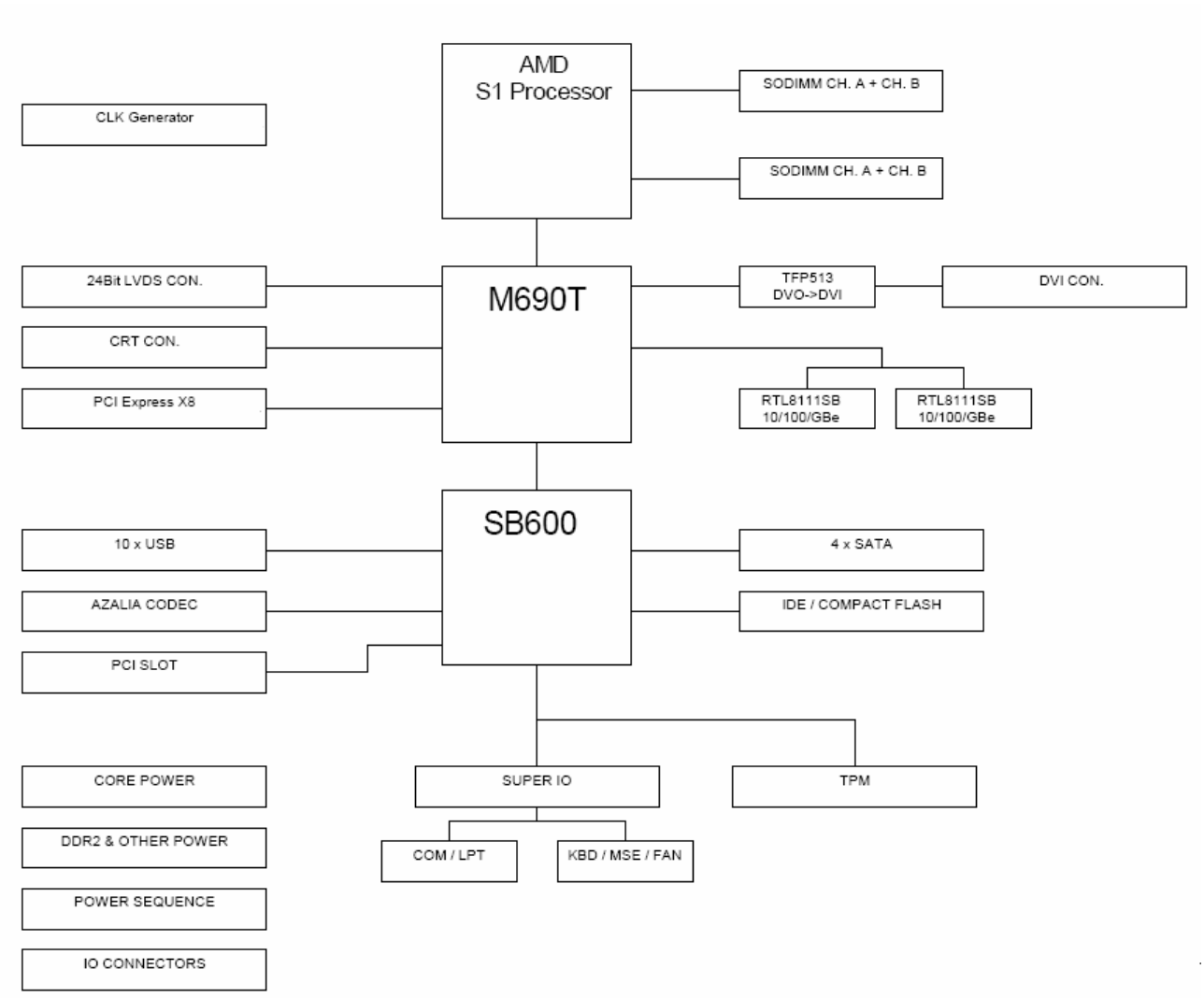
I/O Control	Winbond W83627DHG LPC Bus I/O Controller
Peripheral interfaces	• Six USB 2.0 ports on I/O area • Four USB 2.0 ports on internal pinrows • Two Serial ports (RS232) • One Parallel port, SPP/EPP/ECP • One Floppy port • Four Serial ATA-300 IDE interfaces • One PATA ultra DMA 33/66/100/133 MHz channel • PS/2 keyboard and mouse ports
LAN Support	• 2x 10/100/1000Mbits/s LAN using Realtek RTL8111B controllers • RPL/PXE netboot supported. Wake On LAN (WOL) supported.
BIOS	• Kontron Technology / AMI BIOS (core version) • Support for Advanced Configuration and Power Interface (ACPI 1.0b), Plug and Play o Suspend To Ram o Suspend To Disk • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • RAID Support (RAID modes 0, 1, and 10) (for Linux O/S limitations may apply)
Expansion Capabilities	• PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.3) o KT690/mITX: 1 slot PCI 2.3, 32 bits, 33 MHz, 5V compliant • PCI-Express bus routed to PCI Express slot(s) (PCI Express 1.1a) o KT690/mITX: 1 slot PCI-Express x16 with PCI-Express x8 support o ADD2 / SDVO not supported • Mini PCI-Express routed to mini PCI-Express connector Support for Mini PCI-Express modules with no components on backside. • SMBus routed to FEATURE, PCI slot, PCI Express and mini-PCI Express connectors • LPC Bus routed to TPM connector • DDC Bus routed to LVDS and CRT connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_CPU, FAN_SYS and FEATURE • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 3ºC) • Voltage monitoring • Intrusion detect input • SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• Win2000 • WinXP • Windows Vista • WinXP Embedded (limitations may apply) • Linux: Fedora Core 8 (limitations may apply)

(continues)

Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition, **Approval pending** CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** TBD **Restriction of Hazardeous Substances (RoHS):** All boards in the KT690 family are RoHS compliant. **Capacitor utilization:** No Tantal capacitors on board Only Japanese brand Aluminium and solid electrolytic capacitors rated for 100degrees Celsius used on board
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR2032. Approximate 5 years retention. Current draw is 3µA when PSU is disconnected. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

3.2 System overview

The block diagram below shows the architecture and main components of the KT690 board. The two key components on the board are the AMD® M690T and AMD® SB600 Embedded Chipsets.



3.3 Processor support table.

The KT690 is designed to support the following socket S1 processors:

Mobile AMD Sempron™

AMD Turion™ 64 Mobile Processors

AMD Turion™ 64 X2 Mobile Processors

Processor Brand	Clock Speed [MHz]	Core]	Order Number	Thermal Guideline [Watt]	Embedded
Mobile AMD Sempron	1600	Single	SMS3200HAX4CM	25	
Mobile AMD Sempron	1800	Single	SMS3400HAX3CM	25	
Mobile AMD Sempron	1800	Single	SMS3500HAX4CM	25	
Mobile AMD Sempron	2000	Single	SMS3600HAX3CM	25	
Mobile AMD Turion 64	2000	Single	TMDMK36HAX4CM	35	
Mobile AMD Turion 64 X2	1600	Dual	TMDTL50HAX4CT	31	
Mobile AMD Turion 64 X2	1600	Dual	TMDTL52HAX5CT	31	
Mobile AMD Turion 64 X2	1800	Dual	TMDTL56HAX5CT	33	
Mobile AMD Turion 64 X2	2000	Dual	TMDTL60HAX5CT	35	
Mobile AMD Turion 64 X2	2200	Dual	TMDTL64HAX5CT	35	

3.4 KT690 Power State Map

POWER NET/STATE	S0#	S3#	S5#
+3V3	ON	OFF	OFF
+5V	ON	OFF	OFF
+12V	ON	OFF	OFF
-12V	ON	OFF	OFF
+VCORE	ON	OFF	OFF
+0V9_SUS	ON	ON	OFF
+1V2	ON	OFF	OFF
+1V2_CPU	ON	OFF	OFF
+1V8_SUS	ON	ON	OFF
+2V5_CPU_VDDA	ON	OFF	OFF
+3V3_CLK	ON	OFF	OFF
+3V3_DUAL	ON	ON	ON
+1V8	ON	OFF	OFF
+5V_DUAL	ON	ON	ON
+3V3_ETH1	ON	(ON)	(ON)
+3V3_ETH2	ON	(ON)	(ON)
+V_BAT	ON	ON	ON
+1V2_DUAL	ON	ON	ON
+5V_ALWAYS	ON	ON	ON
+2V5	ON	OFF	OFF
+1V5	ON	OFF	OFF

4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

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The connector definitions follow the following notation:

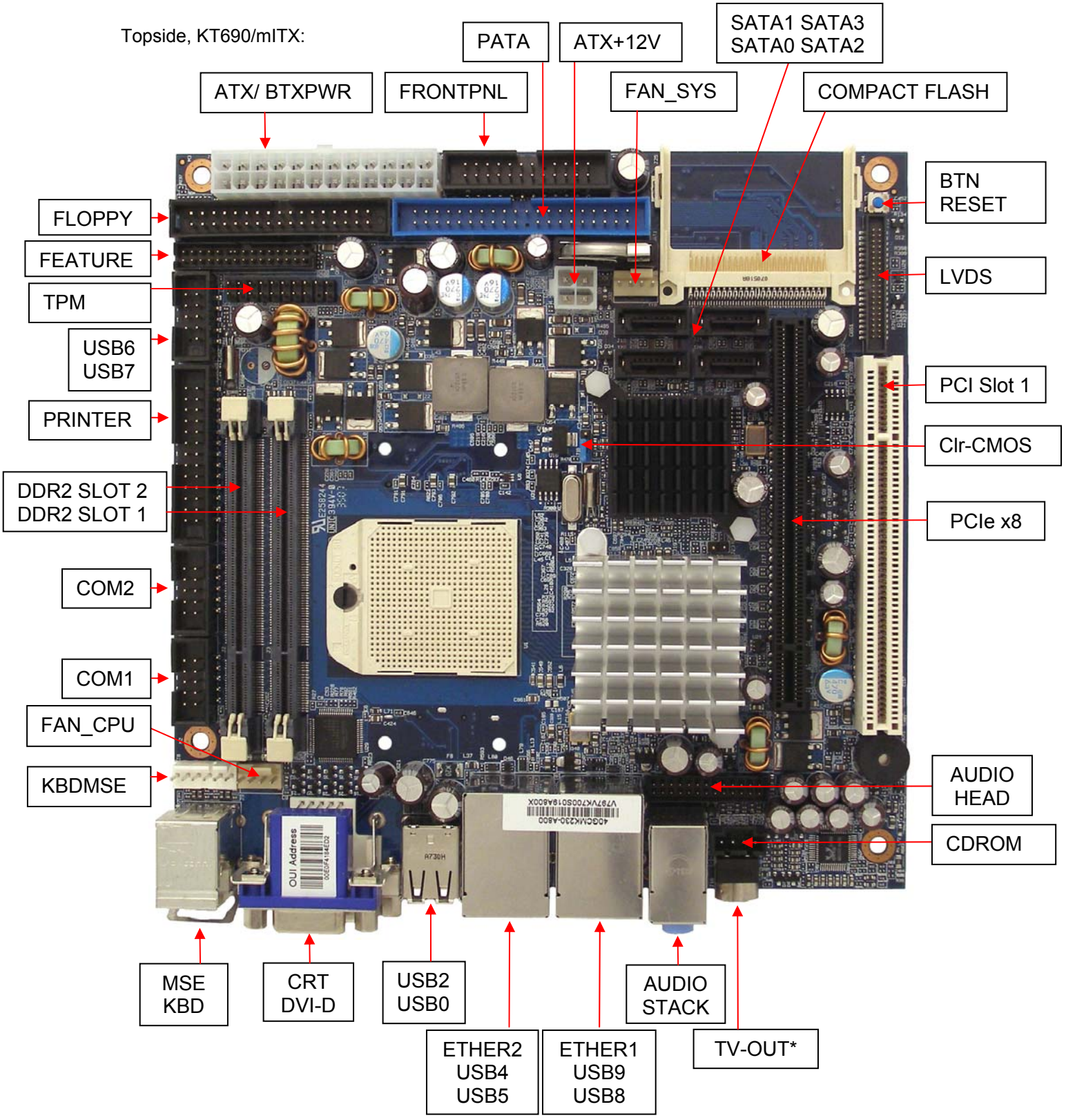
Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

4.1 Connector layout

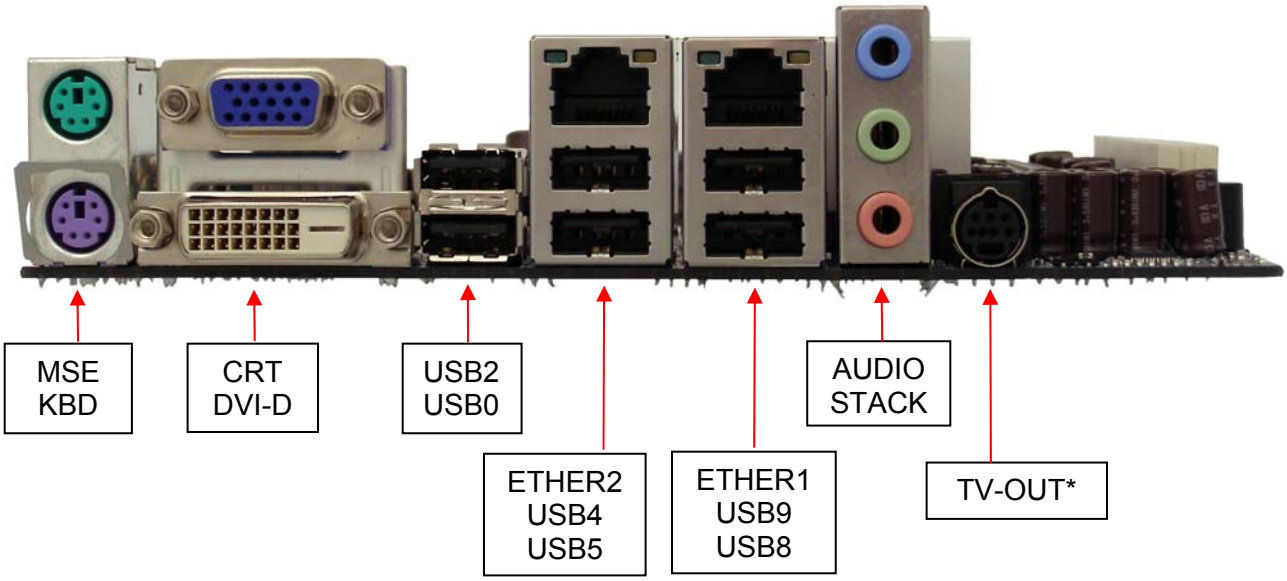
4.1.1 KT690/mITX

Topside, KT690/mITX:



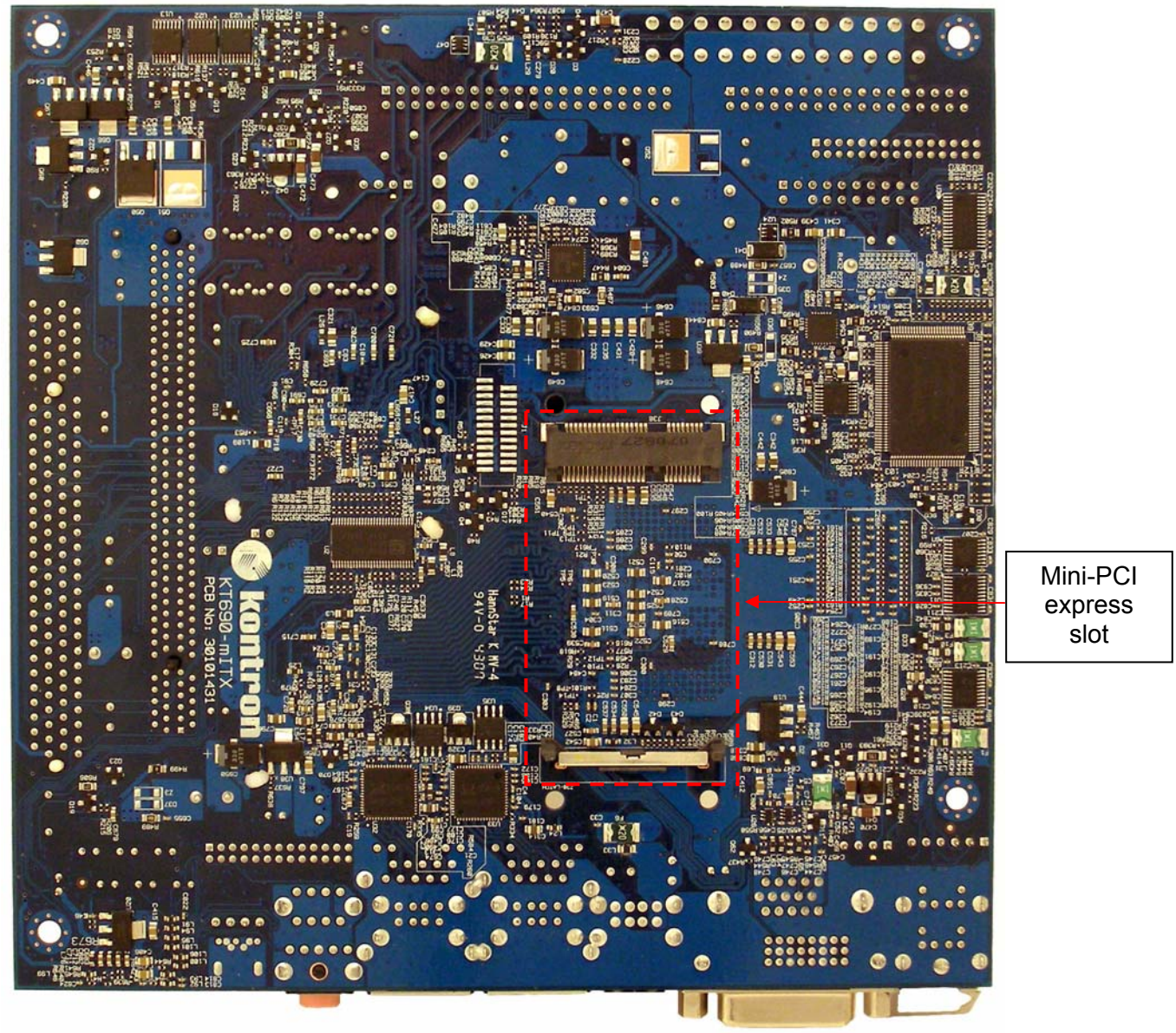
* Mounted optionally

Front, KT690/mITX



* Mounted optionally

Backside, KT690/mITX:



4.2 Power Connector (ATXPWR)

The KT690 boards are designed to be supplied from a standard ATX or BTX power supply.

ATX/ BTX Power Connector:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	3V3	12	24	GND	PWR	-	-	
			PWR	+12V	11	23	5V	PWR			
			PWR	+12V	10	22	5V	PWR			
	-	-	PWR	SB5V	9	21	5V	PWR	-	-	
	-	-	I	P_OK	8	20	-5V	PWR	-	-	1
	-	-	PWR	GND	7	19	GND	PWR	-	-	
	-	-	PWR	5V	6	18	GND	PWR	-	-	
	-	-	PWR	GND	5	17	GND	PWR	-	-	
	-	-	PWR	5V	4	16	PSON#	OC	-	-	
	-	-	PWR	GND	3	15	GND	PWR	-	-	
	-	-	PWR	3V3	2	14	-12V	PWR	-	-	
	-	-	PWR	3V3	1	13	3V3	PWR	-	-	

Note 1: -5V supply is not used onboard.
Note 2: Use of BTX supply not required for operation, but may be required to drive high-power PCI Express x16 Add cards.

ATX+12V Power Connector:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	GND	1	3	+12V	PWR	-	-	1
1			PWR	GND	2	4	+12V	PWR			1

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of the KT690 boards.

See chapter “Power Consumption” regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

Control signal description:

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply with the KT690 boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the KT690 boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOC	TBD	2K7	
			-	NC	6 5	KBDCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOC	TBD	2K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 Keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	4K7	
2	KBDDAT	IOC	TBD	4K7	
3	MSCLK	IOC	TBD	4K7	
4	MSDAT	IOC	TBD	4K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

4.4 Display Connectors

The KT690 board provides:

1. Analog CRT interface (Front panel)
2. Digital DVI (DVI-D) (Front panel)
3. LVDS connector (internal connector)
4. TV-Out (Front)

The KT690 board does not support ADD2 / SDVO cards on the PCI Express x16 connector.

The KT690 integrates the ATI Radeon™ X1250 Graphics Core with support for Dual Clone display and Dual independent display.

The supported combinations are listed in the below matrix:

		Primary Display			
		CRT	**DVI-D**	**LVDS**	**TV-Out**
Secondary Display	**CRT**		Clone / Dual	Clone / Dual	TBD
	DVI-D	Clone / Dual		Clone / Dual	TBD
	LVDS	Clone / Dual	Clone / Dual		TBD
	TV-Out	TBD	TBD	TBD	

TBD: To be determined.

4.4.1 CRT Connector (CRT)

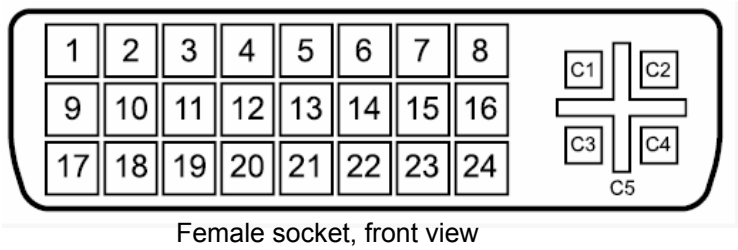
Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	6K81	2
						8		GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		GND	PWR	-	-	
	-	-	PWR	GND	5		15	DDCCLK	IO	TBD	6K81	2

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.
Note 2: Pull-up to +5V.

Signal Description - CRT Connector:

Signal	Description
HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

4.4.2 DVI Connector (DVI-D, digital only)



Female socket, front view

Note 1: Pins C1-C5 (DVI analogue signals) are not supported, but may be present for compatibility.

Signal Description - DVI Connector:

Pin No.	Signal	Description	Type	Pull Up
1	TMDS Data 2-	Digital Red – (Link 1)	LVDS OUT	
2	TMDS Data 2+	Digital Red + (Link 1)	LVDS OUT	
3	TMDS Data 2/4 Shield		PWR	
4	N.C.		-	
5	N.C.		-	
6	DDC Clock	DDC Clock	IO	2K2
7	DDC Data	DDC Data	IO	2K2
8	N.C.		-	
9	TMDS Data 1-	Digital Green – (Link 1)	LVDS OUT	
10	TMDS Data 1+	Digital Green + (Link 1)	LVDS OUT	
11	TMDS Data 1/3 Shield		PWR	
12	N.C.		-	
13	N.C.		-	
14	+5V (55mA)	Power for monitor when in standby	PWR	
15	GND		PWR	
16	Hot Plug Detect	Hot Plug Detect	I	
17	TMDS Data 0-	Digital Blue – (Link 1) / Digital sync	LVDS OUT	
18	TMDS Data 0+	Digital Blue + (Link 1) / Digital sync	LVDS OUT	
19	TMDS Data 0/5 Shield		PWR	
20	N.C.		-	
21	N.C.		-	
22	TMDS Clock Shield		PWR	
23	TMDS Clock+	Digital clock + (Link 1)	LVDS OUT	
24	TMDS Clock-	Digital clock - (Link 1)	LVDS OUT	
C1 - C5	N.C.		-	

4.4.3 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	Pin		Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
2K2Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	2K2Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Note 1: The KT690 board support dual channel, 24bit OpenLDI/ SPWG panels on the LVDS interface

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0..B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock
DDC DATA	DDC Channel Data

Note 1) Windows API will be available to operate the BKLTCTL signal. Some Inverters has a limited voltage range 0- 2.5V for this signal: If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise to the BKLTCTL signal resulting in making the lvds transmision fail (corrupted picture on the display). By adding 1K Ohm resistor in series with this signal and mounted in the Inverter end of the cable kit the noise is limited and picture is stabil.

Note 2) If the Backlight Enable is required to be active high then make the BIOS Chipset setting: Backlight Signal Inversion = Enabled.

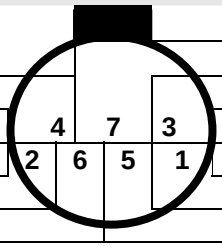
4.4.4 TV-Out (Not supported)

The KT690 boards include TV-Out connector with support for Component, S-Video and Composite Output interfaces and NTSC/ PAL output format.

The KT690 board includes Macrovision support.

IMPORTANT: If the TV-Out option is available then you must make agreement with Macrovision (http://www.macrovision.com/) about licence fee. Only Macrovision (not Kontron) can determine the actual licence fee which depends on the application.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
						GND				
				TVDACC		TVDACB				
					4 7 3					
					2 6 5 1					
				GND		GND				
				GND		TVDACA				



Signal	Description
TVDACA	TVDAC Channel A output supports: Composite: CVBS signal Component: Chrominance (Pb) analog signal
TVDACB	TVDAC Channel B output supports: S-Video: Luminance analog signal Component: Luminance (Y) analog signal
TVDACC	TVDAC Channel C output supports: S-Video: Chrominance analog signal Component: Chrominance (Pr) analog signal

4.5 PCI-Express Connectors

The KT690 board contains one 8-lane (x8) PCI Express port on a PCI Express x16 connector. The PCI Express port is compliant to the PCI Express Specification revision 1.1a.

The x8 port operates at a frequency of 2.5 Gb/s on each lane; the port supports a maximum theoretical bandwidth of 20 Gb/s in each direction.

The 8-lane (x8) PCI Express port supports:

1. An external graphics device utilizing all 8 lanes
2. A single x1, x2 or x4 general purpose PCI Express link

The PCI Express port does not support SDVO and ADD2 cards.

4.5.1 PCI-Express x8

The KT690 boards supports one 8-lane (x8) PCI Express port for external PCI Express based graphics boards.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[0]	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[0]	B15	A15	GND		
		GND	B16	A16	PEG_RXP[0]		
		I2C_CLK	B17	A17	PEG_RXN[0]		
		GND	B18	A18	GND		
		PEG_TXP[1]	B19	A19	NC		
		PEG_TXN[1]	B20	A20	GND		
		GND	B21	A21	PEG_RXP[1]		
		GND	B22	A22	PEG_RXN[1]		
		PEG_TXP[2]	B23	A23	GND		
		PEG_TXN[2]	B24	A24	GND		
		GND	B25	A25	PEG_RXP[2]		
		GND	B26	A26	PEG_RXN[2]		
		PEG_TXP[3]	B27	A27	GND		
		PEG_TXN[3]	B28	A28	GND		
		GND	B29	A29	PEG_RXP[3]		
		NC	B30	A30	PEG_RXN[3]		
		DDC_DATA	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[4]	B33	A33	NC		
		PEG_TXN[4]	B34	A34	GND		
		GND	B35	A35	PEG_RXP[4]		
		GND	B36	A36	PEG_RXN[4]		
		PEG_TXP[5]	B37	A37	GND		
		PEG_TXN[5]	B38	A38	GND		
		GND	B39	A39	PEG_RXP[5]		
		GND	B40	A40	PEG_RXN[5]		
		PEG_TXP[6]	B41	A41	GND		
		PEG_TXN[6]	B42	A42	GND		
		GND	B43	A43	PEG_RXP[6]		
		GND	B44	A44	PEG_RXN[6]		
		PEG_TXP[7]	B45	A45	GND		
		PEG_TXN[7]	B46	A46	GND		
		GND	B47	A47	PEG_RXP[7]		

(continues)

		PRSNT#2	B48	A48	PEG_RXN[7]		
		GND	B49	A49	GND		
		NC	B50	A50	NC		
		NC	B51	A51	GND		
		GND	B52	A52	NC		
		GND	B53	A53	NC		
		NC	B54	A54	GND		
		NC	B55	A55	GND		
		GND	B56	A56	NC		
		GND	B57	A57	NC		
		NC	B58	A58	GND		
		NC	B59	A59	GND		
		GND	B60	A60	NC		
		GND	B61	A61	NC		
		NC	B62	A62	GND		
		NC	B63	A63	GND		
		GND	B64	A64	NC		
		GND	B65	A65	NC		
		NC	B66	A66	GND		
		NC	B67	A67	GND		
		GND	B68	A68	NC		
		GND	B69	A69	NC		
		NC	B70	A70	GND		
		NC	B71	A71	GND		
		GND	B72	A72	NC		
		GND	B73	A73	NC		
		NC	B74	A74	GND		
		NC	B75	A75	GND		
		GND	B76	A76	NC		
		GND	B77	A77	NC		
		NC	B78	A78	GND		
		NC	B79	A79	GND		
		GND	B80	A80	NC		
		NC	B81	A81	NC		
		NC	B82	A82	GND		

4.5.2 miniPCI-Express connector

The KT690 board supports one miniPCI Express port compliant to the Mini PCI Specification, Revision 1.0.
This allows for implementation for small form factor PCI cards also referred to as Mini PCI Cards.

Note	Type	Signal	PIN		Signal	Type	Note
		WAKE#	1	2	+3V3		
		NC	3	4	GND		
		NC	5	6	+1.5V		
		NC	7	8	NC		
		GND	9	10	NC		
		PCIE_mini CLK#	11	12	NC		
		PCIE_mini CLK	13	14	NC		
		GND	15	16	NC		
		NC	17	18	GND		
		NC	19	20	W_Disable		
		GND	21	22	RST#		
		PCIE_RXN	23	24	+3V3		
		PCIE_RXP	25	26	GND		
		GND	27	28	+1.5V		
		GND	29	30	SMB_CLK		
		PCIE_TXN	31	32	SMB_DATA		
		PCIE_TXP	33	34	GND		
		GND	35	36	NC		
		NC	37	38	NC		
		NC	39	40	GND		
		NC	41	42	NC		
		NC	43	44	NC		
		NC	45	46	NC		
		NC	47	48	+1.5V		
		NC	49	50	GND		
		NC	51	52	+3V3		

4.6 Parallel ATA harddisk interface

One parallel ATA harddisk controllers is available on the board – a primary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller by means of the 40 pin IDC connector, PATA.

The parallel ATA harddisk controller is shared between the PATA connector and the CF connector. If the CF connector is used only one PATA disk is supported. If the CF connector is not used, a primary and a secondary harddisk is supported on the PATA interface.

The harddisk controllers support Bus master IDE, ultra DMA 33/66/100/133 MHz and standard operation modes. For support of ultra DMA 66/100/133 MHz, a 80 wire cable is required.

The signals used for the harddisk interface are the following:

Signal	Description
DAA2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCSA1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
DA15..8	High part of data bus.
DA7..0	Low part of data bus.
IORA#	I/O Read.
IOWA#	I/O Write.
IORDYA#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESETA#	Reset signal to the hard disk.
HDIRQA	Interrupt line from hard disk.
CBLIDA	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQA	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACKA#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACTA#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].
The pinout of the connectors are defined in the following sections.

4.6.1 IDE Hard Disk Connector (PATA)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESET_P#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

4.6.2 CF Connector (CF)

This connector is mounted on the topside of the KT690/mITX. If a Compact Flash Disk is used, only one PATA drive can be connected to the PATA connector. The CF socket support DMA/UDMA modules.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	-	-	NC	26	1	GND	PWR	-	-	1
	-	TBD	IO	DA11	27	2	DB3	IO	TBD	-	
	-	TBD	IO	DA12	28	3	DB4	IO	TBD	-	
	-	TBD	IO	DA13	29	4	DB5	IO	TBD	-	
	-	TBD	IO	DA14	30	5	DB6	IO	TBD	-	
	-	TBD	IO	DA15	31	6	DB7	IO	TBD	-	
	-	TBD	O	HDCSA1#	32	7	HDCSA0#	O	TBD	-	
	-	-	-	NC	33	8	GND	PWR	-	-	
	-	TBD	O	IORA#	34	9	GND	PWR	-	-	
	-	TBD	O	IOWA#	35	10	GND	PWR	-	-	
	-	-	PWR	5V	36	11	GND	PWR	-	-	
	8K2	-	I	HDIRQA	37	12	GND	PWR	-	-	
	-	-	PWR	5V	38	13	5V	PWR	-	-	
	-	-	PWR	GND	39	14	GND	PWR	-	-	
	-	-	-	NC	40	15	GND	PWR	-	-	
	-	TBD	O	RESET_C#	41	16	GND	PWR	-	-	
	4K7	-	I	IORDYA	42	17	GND	PWR	-	-	
	-	-	I	DDRQA	43	18	DAA2	O	-	-	
	-	-	O	DDACKA#	44	19	DAA1	O	-	-	
	-	-	I	HDACTA#	45	20	DAA0	O	-	-	
	-	-	I	CBLIDA#	46	21	DB0	IO	TBD	-	
	-	TBD	IO	DB8	47	22	DB1	IO	TBD	-	
	-	TBD	IO	DB9	48	23	DB2	IO	TBD	-	
	-	TBD	IO	DB10	49	24	NC				
1	-	-	PWR	GND	50	25	NC	-	-	-	2

Note 1: Pin is longer than average length of the other pins.
Note 2: Pin is shorter than average length of the other pins.

4.7 Serial ATA harddisk interface

The KT690 boards have an integrated SATA Host controller that supports independent operation on four ports and data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0, 1 and 10.

The board provides four Serial ATA (SATA) connectors, which support one device per connector.
The SB600 Southbridge Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port.
A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.
For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows 2000 operating systems.

The KT690 supports the following RAID (Redundant Array of Independent Drives) levels:
- RAID 0 - data striping
- RAID 1 - data mirroring
- RAID 0+1 (or RAID 10) - data striping and mirroring

Limitations depending on Target Operating System apply.

4.7.1 SATA Hard Disk Connector (SATA0, SATA1, SATA2, SATA3)

SATA:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

"*" specifies 0, 1, 2, and 3 depending on SATA port.
All of the above signals are compliant to [4].

4.8 Printer Port Connector (PRINTER).

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3	4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11	12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13	14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15	16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17	18	GND	PWR	-	-	
	2K2	-	I	ACK#	19	20	GND	PWR	-	-	
	2K2	-	I	BUSY	21	22	GND	PWR	-	-	
	2K2	-	I	PE	23	24	GND	PWR	-	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

4.9 Floppy connector (FLOPPY).

The KT690 supports connection of one standard 1.44M Floppy device.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	1	2	DENSEL0#	OC	/48	-	
	-	-	PWR	GND	3	4	NC	-	-	-	
	-	-	PWR	GND	5	6	NC	-	-	-	
	-	-	PWR	GND	7	8	INDEX#	IS	-	330R	
	-	-	PWR	GND	9	10	MOTEA#	OC	/48	-	
	-	-	PWR	GND	11	12	NC	OC	/48	-	
	-	-	PWR	GND	13	14	DRVA#	OC	/48	-	
	-	-	PWR	GND	15	16	NC	OC	/48	-	
	-	-	PWR	GND	17	18	DIR#	OC	/48	-	
	-	-	PWR	GND	19	20	STEP#	OC	/48	-	
	-	-	PWR	GND	21	22	WDATA#	OC	/48	-	
	-	-	PWR	GND	23	24	WGATE#	OC	/48	-	
	-	-	PWR	GND	25	26	TRK0#	IS	-	330R	
	-	-	PWR	GND	27	28	WPT#	IS	-	330R	
				NC	29	30	RDATA#	IS	-	330R	
	-	-	PWR	GND	31	32	SIDE1#	OC	/48	-	
				NC	33	34	DSKCHG#	IS	-	330R	

Signal Description:

RDATA#	Read Disk Data, active low, serial data input from the floppy disk drive.
WDATA#	Write Disk Data, active low, serial data output to the floppy disk drive.
WGATE#	This output signal enables the head of the selected disk drive to write to the disk.
MOTEA#	This output signal enables the motor in floppy disk drive A.
DRVA#	Active low output signal to select floppy disk drive A.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	This signal controls the direction of the floppy disk drive head movement during a seek operation. A low level request steps through centre.
STEP#	This output signal supplies step pulses to move the head during seek operations.
DENSEL0#	This output indicates whether a low data rate (250/300kbps at low level) or a high data rate (500/1000kbps at high level) has been selected.
TRK0#	Floppy Disk Track 0, active low input to indicate that the head of the selected drive is at track 0.
INDEX#	Floppy Disk Index, active low input indicates the beginning of a disk track.
WPT#	Active low input signal indicating that the selected drive contains a write protected disk.
DSKCHG#	Input pin that senses whether the drive door has been opened or the diskette has been changed.

4.10 Serial Ports

Two RS232 serial ports are available on the KT690/mITX boards

The typical interpretation of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.10.1 Com1 Pin Header Connector.

The pinout of Serial ports Com1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The Com1 header 5V supply is fused with a 1.1A resetable fuse.

A DB9 adapter (ribbon cable) can be used to make a DB9 pinout available.

4.10.2 Com2 Pin Header Connector.

The pinout of Serial ports Com2 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The Com2 header 5V supply is fused with a 1.1A resetable fuse.

A DB9 adapter (ribbon cable) can be used to make a DB9 pinout available.

4.11 Ethernet connectors.

The KT690/mITX boards supports 2 channels of 10/100/1000Mb Ethernet RTL8111B LAN controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[0]-	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]-	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDI[2]-	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDI[3]-	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

4.11.1 Ethernet connector 1 (ETHER1)

Ethernet connector 1 is mounted together with USB Ports 8 and 9.

The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2-				
MDI1-				
MDI2+				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

4.11.2 Ethernet connector 2 (ETHER2)

Ethernet connector 2 is mounted together with USB Ports 4 and 5.

The pinout of the RJ45's connector are as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2-				
MDI1-				
MDI2+				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

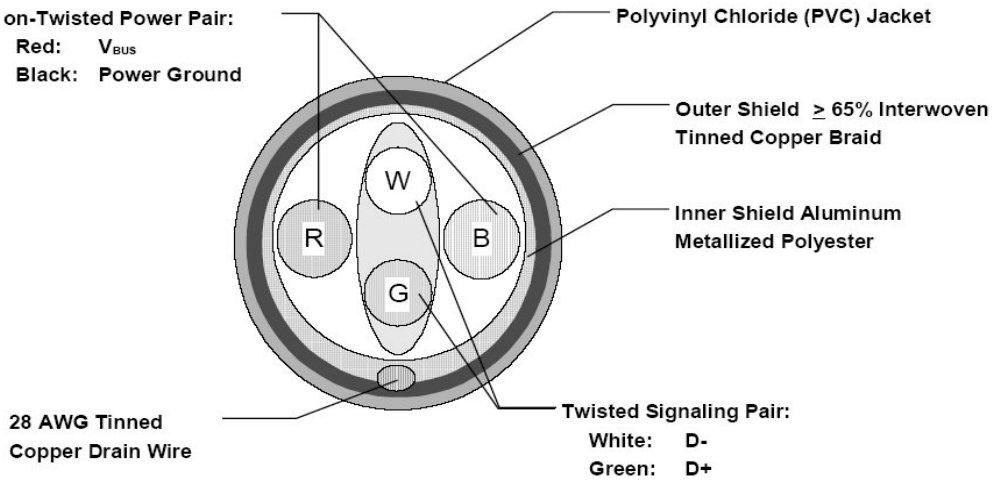
4.12 USB Connector (USB)

The KT690 boards contains one Enhanced Host Controller Interface (EHCI) host controllers that supports USB 2.0 allowing data transfers up to 480Mb/s. The KT690 boards also contains five Open Host Controller Interface (OHCI) controllers that support USB full-speed and low-speed signaling (USB 1.1).
The KT690 boards supports a total of ten USB 2.0 ports. All ten ports are high-speed (USB 2.0), full-speed (USB 1.1), and low-speed (USB 1.1) capable and USB Legacy mode is supported.

Over-current detection on all ten USB ports is supported.

USB Port 0 and 2 are supplied on the USB0, USB2 frontpanel connector.
USB Ports 1 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.
USB Port 4 and 5 are supplied on the combined ETHER2, USB4, USB5 connector.
USB Port 6 and 7 are supplied on the internal USB6, USB7 pinrow connector.
USB Port 8 and 9 are supplied on the combined ETHER1, USB8, USB9 connector.

Note: It is recommended to use only High-/Full-Speed USB cable, specified in USB2.0 standard:



4.12.1 USB Connector 0/2 (USB0/2)

USB Ports 0 and 2 are supplied on the USB0, USB2 frontpanel connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB2+ USB2-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.2 USB Connector 4/5 (USB4/5)

USB Ports 4 and 5 are are supplied on the combined ETHER2, USB4, USB5 connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.3 USB Connector 6/7 (USB6/7)

USB Ports 6 and 7 are are supplied on the internal USB6, USB7 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB6-	3	4	USB7-	IO		-	
	-		IO	USB6+	5	6	USB7+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Signal	Description
USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

4.12.4 USB Connector 8/9 (USB8/9)

USB Ports 8 and 9 are supplied on the combined ETHER1, USB8, USB9 connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB9-		USB9+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB8-		USB8+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB8+ USB8- USB9+ USB9-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.13 Audio Connector

The onboard Audio circuit implements 7.1+2 Channel High Definition Audio, featuring ten 24-bit stereo DACs and two 20-bit stereo ADCs.
Thew Audio signals are made available on the Frontpanel stacked connector (Line in / Line out / MIC) and the onboard AUDIO_HEAD and CDROM Audioinput connectors.

4.13.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector.

IN	Signal	Type	Note
TIP	LINE1-IN-L	IA	1
RING	LINE1-IN-R	IA	1
SLEEVE	GND	PWR	
TIP	FRONT-OUT-L	OA	
RING	FRONT-OUT-R	OA	
SLEEVE	GND	PWR	
TIP	MIC1-L	IA	1
RING	MIC1-R	IA	1
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

4.13.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

4.13.3 AUDIO Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

4.14 Fan connectors , FAN_CPU and FAN_SYS.

The **FAN_CPU** is used for connection of the active cooler for the CPU.
The **FAN_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.

The 4pin header supports connection of 3-pin FANs, but it is recommended to use the 4-pin type for optimized FAN speed control. The 3- or 4-pin mode is controlled in the BIOS setup menu.

4-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CONTROL	O	-	-	
2	SENSE	I	-	-	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal description:

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

3-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
2	SENSE	I	-	-	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal description:

Signal	Description
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

4.15 The Clear CMOS Jumper, Clr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.

↑ CPU location ↑

No Jumper installed

(Pin numbers)

Jumper normal position

Jumper in Clear CMOS position

To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

4.16 TPM connector (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	LPC IRQ#				

4.17 Front Panel connector (FRONTPNL).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				USB13_5V	1	2	USB13_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	KEY		10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
1				MIC2-L	23	24	MIC2-R				1

Note 1: Unsupported inputs, leave these inputs unconnected.

Signal	Description
USB13_5V	+5V supply for the USB devices on USB Port 1 and 3 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connectorfladkabel or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for minimum 16mS the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R are unsupported. Leave these terminals unconnected.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

4.18 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I			
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
1	4K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	2K7/	1
1	4K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	2K7/	1
1	4K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	2K7/	3
3	4K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	2K7/	3
	-	-	PWR	GND	19	20	FAN3OUT				
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Note 1: Pull-up to +3V3Dual (+3V3 or SB3V3). Note 2: Pull-up to RTC-Voltage. Note 3: Pull-up to +3V3.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND (etc. pin 10). The external battery is protected against charging and can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC. Current draw is 3µA when PSU is disconnected.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KONTRON API (Application Programming Interface) available for WinXP and Win2000.
FAN3OUT	FAN 3 speed control OUTput. This analogue voltage output signal can be set to output voltages from 0 – 3V3 to control the Fan's speed.. For more information please look into the datasheet for the Winbond I/O controller W83627.
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin23 (Temp3-In). Further a resistor 30K/1% shall be connected between pin 23 and pin 24 (Vref). (Precision +/- 3ºC)
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

4.19 PCI Slot Connector

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
		NC	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
		NC	F09	E09	NC		
		NC	F10	E10	+5V (I/O)	PWR	
		NC	F11	E11	NC	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
		NC	F14	E14	3V3	OT	
	PWR	GND	F15	E15	RST#	O	
	O	PCICLK	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	O	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	IDSEL	IOT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SMB_CLK	IO	
	PWR	+3.3V	F41	E41	SMB_DATA	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE				**COMPONENT SIDE**			
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
8K2/ PU	IOT	ACK64#	F60	E60	REQ64#	IOT	8K2/ PU
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

4.19.1 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(continues)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

4.19.2 KT690 PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
KT690/mITX	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E. 820982 PCI Riser shall be plugged into Slot #1.

5. Onboard Connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_SYS, FAN_CPU	Molex	22-23-2031	AMP	1375820-3
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA0-3	Molex	67491-0020	Molex	67489-8005
			Kontron	KT 821035 (cable kit)
ATXPWR	Foxconn	HM2510E	Molex	39-01-2205
COM1 + COM2	Foxconn	HL20051	Molex	90635-1103
			Kontron	KT 821016 (cable kit)
			Kontron	KT 821017 (cable kit)
USB6 USB7	Foxconn	HC11051-P9	Kontron	KT 821401 (cable kit)
PRINTER	Foxconn	HL2213F	Molex	90635-1263
			Kontron	KT 821031 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
FRONTPNL	Foxconn	HL20121	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1
			Kontron	KT 821515 (cable kit)
			Kontron	KT 821155 (cable kit)

6. System Ressources

6.1 Memory map

Address range (hex)	Size	Description

6.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function

When a PCI-E or Mini PCI-E card is used it could change the BUS number on other PCI-E and PCI devices like RTL8111b.
Note: PCI slot supports PCI BUS Mastering.

6.3 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Parallel Port	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used for SATA RAID controller	May be used for onboard Sound System	May be used for PCI Express Root Port	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard VGA Controller	May be used by onboard SMBus Controller	Available on PCI slots as IRQA-IRQD depending on selections in the BIOS	Notes
NMI																				
IRQ0																				
IRQ1																				
IRQ2																				
IRQ3																				1, 2
IRQ4																				1, 2
IRQ5																			•	1, 2
IRQ6																				1, 2
IRQ7																			•	1, 2
IRQ8																				
IRQ9																			•	1, 2
IRQ10																			•	1, 2
IRQ11																			•	1, 2
IRQ12																				1
IRQ13																				
IRQ14																				1
IRQ15																				1
IRQ16																				3
IRQ17																				3
IRQ18																				3
IRQ19																				3
IRQ20																				3
IRQ21																				3
IRQ22																				3
IRQ23																				3
IRQ24																				3
IRQ25																				3
IRQ26																				3

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ16 to IRQ26 are APIC interrupts

6.4 I/O Map

Address (hex)	Size	Description

Notes: This is the IO map after a standard Windows XP SP2 installation

6.5 DMA Channel Usage

DMA Channel Number	Data Width	System Ressources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

7. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.